Neuron® 3150® Chip External Memory Interface

Introduction

The Neuron 3150 Chip provides an external memory bus to permit expansion of memory up to 58K bytes beyond the 512 bytes of EEPROM and 2K bytes of RAM resident on the chip. The Neuron 3150 Chip requires 16K bytes of external non-volatile memory to store its Neuron 3150 Chip Firmware. The remaining 42K bytes of external memory space is available for the application program and data. The external memory may be implemented using various combinations of ROM, EPROM, EEPROM, NVRAM, flash memory and static RAM devices. This engineering bulletin assumes the use of second generation (0.8μ) Neuron 3150 Chips, which have improved timing parameters and better memory interface behavior upon a reset. Second generation chips are distinguished from first generation chips by the suffix B1 (i.e., the MC143150B1 from Motorola, and the TMPN3150B1 from Toshiba).

LonBuilder® 3.0 or NodeBuilder™ 1.0 is required for the support of write operations to flash memory by a Neuron 3150 Chip. Earlier versions of LonBuilder do not support write operations to flash memory.

The focus of this engineering bulletin is the Neuron 3150 Chip memory expansion bus. This bulletin describes the logical functions of the memory interface pins, lists the memory bus timing requirements, and includes several memory design examples. The latest version of this engineering bulletin is kept on Echelon's LonLink™ bulletin board. Information on accessing the LonLink bulletin board is given at the end of this engineering bulletin. Before beginning a new design involving the Neuron 3150 Chip and external memory, engineers should check the LonLink bulletin board to ensure that they have the latest versions of the example memory schematics:

Example 1 - External Memory Interface with 32K x 8 EPROM

Example 2 - External Memory Interface with 32K x 8 EPROM and I/O Expansion

Example 3 - External Memory Interface with 32K x 8 EPROM and 24K x 8 SRAM

Example 4 - External Memory Interface with 32K x 8 Flash Memory

Example 5 - External Memory Interface with 56K x 8 Flash Memory

Example 6 - External Memory Interface with 32K x 8 Flash and 24K x 8 SRAM

Revision History

The original April 1993 revision of the External Memory Interface engineering bulletin contained information on the memory interface for the first generation Neuron 3150 Chip. Special considerations for the behavior of the memory interface of first generation chips after software resets were covered. The memory design examples included EPROM and SRAM only.

Starting with the January 1995 revision of the External Memory Interface engineering bulletin, only second generation (0.8μ) Neuron 3150 Chips were addressed. Four new memory design examples were added, including examples of memory-mapped I/O and flash memory.

This May 1995 revision of the External Memory Interface engineering bulletin has only a few updates from the January 1995 revision. The Atmel flash memory devices specified in this engineering bulletin no longer require an "SL" code to guarantee $t_{DS,min} \leq 35ns$. The example memory schematics have been updated slightly.

Related Documentation

The following Echelon documents are recommended reading:

LonBuilder User's Guide

NodeBuilder User's Guide

Neuron C Programmer's Guide

LonBuilder Startup and Hardware Guide

Neuron Chip Data Book (published by Motorola, Toshiba, and Echelon)

LONWORKS Custom Node Development engineering bulletin

Programmable Peripheral Application Note 025: Interfacing the PSD3xx To The Neuron 3150 Chip (available from Echelon, and published by WSI in their 1994 Data Book, Fremont, CA, phone: 510-656-5400)

Assessing Memory Requirements

LONWORKS devices based on the Neuron 3150 Chip use a combination of three different types of memory:

Non-Volatile Memory for Neuron Chip Firmware: A block of 16K bytes of external non-volatile memory, mapped to 0x0000-0x3FFF, is needed to maintain a permanent copy of the Neuron Chip Firmware.

Non-Volatile Memory for Configuration and Application Information: The Neuron 3150 Chip provides 512 bytes of on-chip EEPROM to store configuration information and the user's application program. EEPROM

technology is used for this memory space since the configuration data, application program and constants can be loaded and modified over the network. External EEPROM, flash memory or non-volatile RAM may be added on the Neuron 3150 Chip memory bus if more space is needed for the application program and constants.

Read/Write Memory for Packet Buffering: The Neuron 3150 Chip contains 2K bytes of on-chip RAM. This internal RAM is used for network packet buffering and for application data space. External RAM may be added to the Neuron 3150 Chip memory bus if more packet buffering or application data space is required. This RAM is assumed to be volatile.

A LONWORKS device may include the external memory types described above by partitioning the available 58K byte memory space into four distinct regions aligned on 256-byte page boundaries. The different memory types do not need to map to contiguous address space. The Neuron C compiler, LonBuilder linker and NodeBuilder linker locate the various parts of an application in the appropriate memory regions.

The LonBuilder and NodeBuilder linkers generate a detailed report of the memory usage in the BUILD.LOG file when the `Output Link Summary` option is enabled.

There are many elements of a LONWORKS application that affect the amount of each type of memory required. Network configuration, the number of network variables, communication buffer parameters, and the amount of application code go into the calculation. As a rule-of-thumb, one can expect roughly six or seven bytes of code per line of Neuron C code. It is always best to create test applications using LonBuilder or NodeBuilder to determine exact requirements.

Echelon's development tools can logically emulate an intended memory configuration to permit evaluation of an application's memory requirements before committing to custom hardware. The LonBuilder and NodeBuilder User's Guides explain how to specify the memory layout of the target node.

The LonBuilder and NodeBuilder linkers determine the appropriate locations for system code, application code, constants and data. These are based on the hardware properties assigned by the system designer, as well as explicit segment definition keywords included in the application code. It is not necessary to create detailed linker command files to map application elements to various memory regions. LonBuilder and NodeBuilder keep track of the necessary details to make correct decisions about memory allocation.

Designs using EEPROM devices must also include a separate EPROM memory to contain the Neuron Chip Firmware. Write cycles to EEPROM memory devices may take up to 20ms to complete, and during this time subsequent read or write cycles accessing the device are blocked. This precludes the use of a single EEPROM memory device to hold the Neuron 3150 Chip Firmware and writeable EEPROM memory, because the Neuron 3150 Chip includes two other active processors which continuously access the same code space as the application processor.   Note that this

limitation does not apply when flash memory is used to store the Neuron 3150 Chip Firmware.

External Memory Design Considerations

The following sections address the logical interfacing and the timing considerations for external memory design.

Memory Interface Logical Description

Figure 1 shows the memory map of the Neuron 3150 Chip. Memory locations from 0x0000 to 0xE7FF are external to the Neuron 3150 Chip. Access to this memory is through an external memory bus consisting of eight bi-directional three-state data lines, 16 unidirectional address lines driven by the Neuron 3150 Chip, and two control lines.
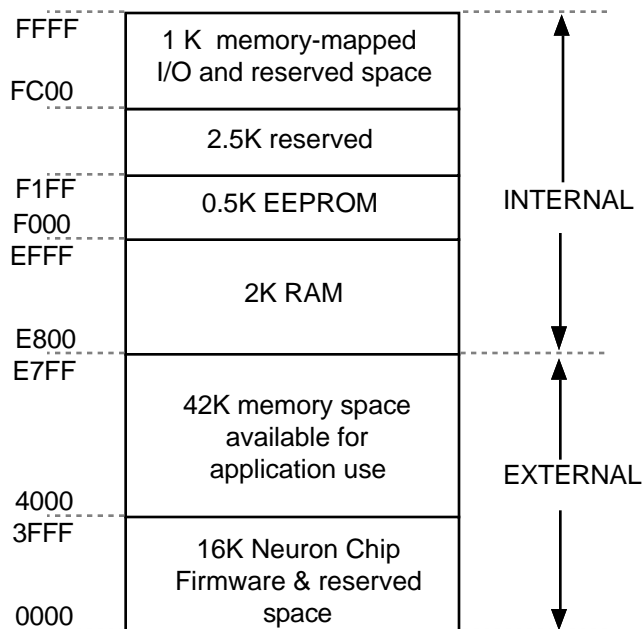

Figure 1 The Neuron 3150 Chip Memory Map

The two control lines used for the external memory interface are:

~E   Enable Clock -- This output is a strobe driven by the Neuron 3150 Chip to synchronize the external bus. Its frequency is one-half that of the input clock or crystal. ~E is low during the second half of the memory cycle, which indicates that the Neuron 3150 Chip is actively reading or writing data. During write cycles, the Neuron 3150 Chip drives the new data onto the data bus during the time ~E is low. For

read cycles, the Neuron 3150 Chip clocks the external data in on the low-to-high transition of ~E.

R/~W   Read/Write -- This output indicates the direction of the data bus. It is high during a Read cycle, and low during a Write cycle. R/~W changes state during the time ~E is high, and is stable during the time ~E is low.

Neuron 3150 Chip Input Loading and Output Drive

The input characteristics of the Neuron 3150 Chip for the memory interface pins are as follows:

Input Voltage levels = TTL

Input current = $\pm$ 10 μA with V_{SS}< V_{IN} < V_{DD}

Note that "V_{DD}" and "Vcc" are used synonymously in this document to refer to the +5V power supply.

All of the Neuron 3150 Chip outputs used for memory interfacing have standard current drive capability, as follows:

V_{OL} = 0.4 V max at I_{OL} = 1.4 mA

V_{OH} = Vdd - 0.4 V min at I_{OH} = -1.4 mA

Timing   Requirements

The Neuron 3150 Chip includes three independent processors sharing a common memory bus. The three processors execute in a pipelined sequence. As a result, the Neuron 3150 Chip can execute a memory operation on every processor cycle. A processor cycle is defined as two input clock periods. Memory wait states are not supported; external memory or memory-mapped I/O devices must respond within the access time dictated by the Neuron 3150 Chip processor cycle time.

Figure 2 and table 1 show the timing for read and write operation of the external memory bus over the operating temperature ranges of the Neuron 3150B1 Chip for $\pm$10% power supply tolerances. Refer to the latest Motorola and Toshiba data sheets for any updates to these timing specifications.
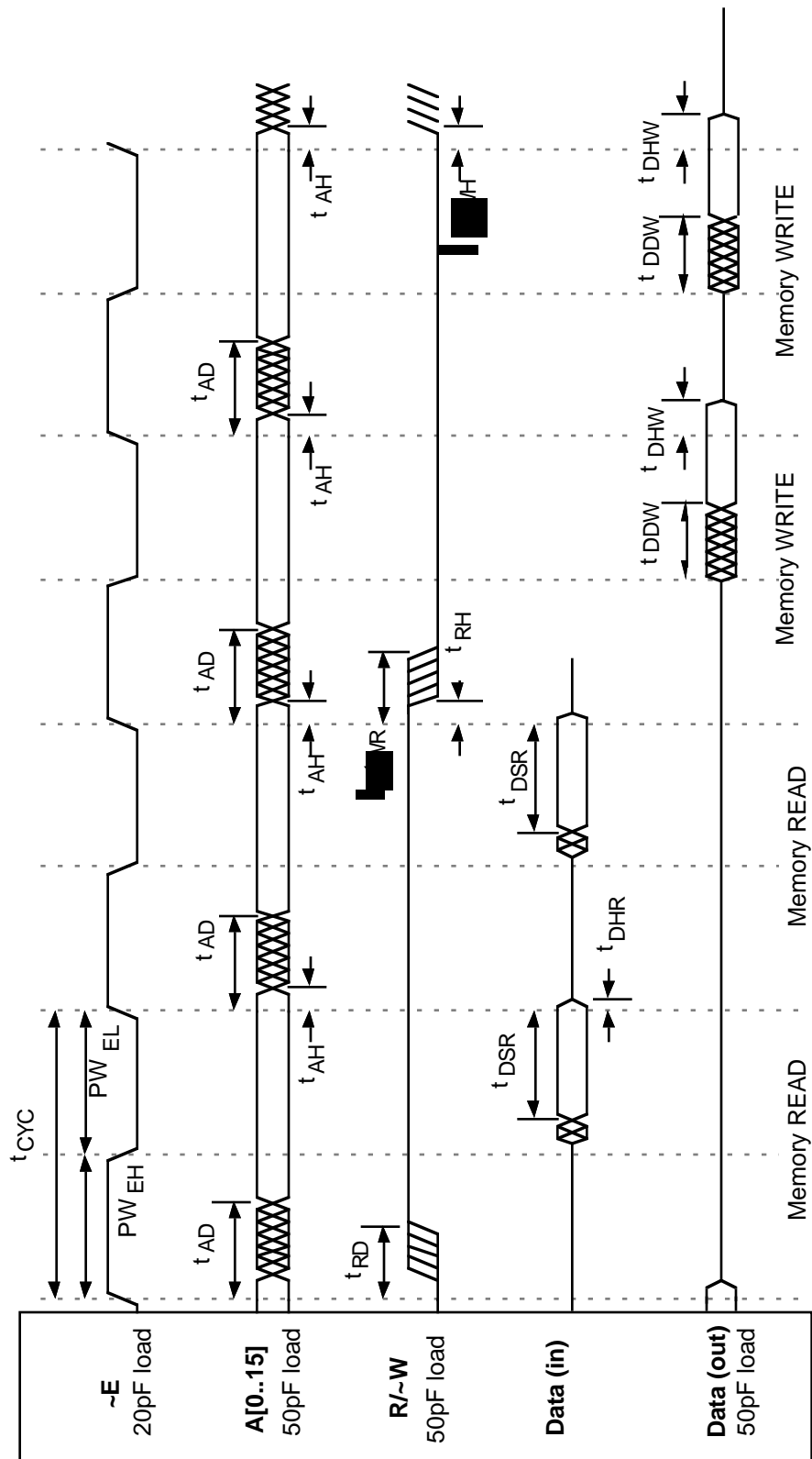
Figure 2   Neuron 3150 Chip Memory Interface Timing Diagram

Table 1   Second Generation (0.8μ) Neuron 3150 Chip Memory Timing
Over ± 10 % Voltage (4.5 to 5.5 V) and Temperature (-40C to +85C)

Symbol	Parameter	Min	Max	Unit
t_{CYC}	Memory cycle time[1]	200	3200	ns
PW_{EH}	Pulse width ~E High	$t_{CYC/2} - 5$	$t_{CYC/2} + 5$	ns
PW_{EL}	Pulse width ~E low	$t_{CYC/2} - 5$	$t_{CYC/2} + 5$	ns
t_{AD}	Delay, ~E High to address valid	-	45	ns
t_{AH}	Address hold time	10	-	ns
t_{RD}	Delay, ~E high to R/~W valid (read operation)	-	25	ns
t_{RH}	R/~W hold time (read operation)	5	-	ns
t_{DSR}	Read data setup time	25	-	ns
t_{DHR}	Data hold time (read operation)	0	-	ns
t_{WR}	Delay, ~E high to R/~W valid (write operation)	-	25	ns
t_{WH}	R/~W hold time (write operation)	5	-	ns
t_{DDW}	Delay, ~E Low to data valid	-	60	ns
t_{DHW}	Data hold time (write operation)	9	40	ns

Notes:

1. $t_{CYC} = 2 \times 1/f$, where 'f' is the input clock frequency at CLK1. Valid values of 'f' are 10, 5, 2.5, 1.25, and 0.625 MHz.

2. These are the preliminary timing parameters for second generation (0.8μ) Neuron 3150B1 Chips. Consult the latest data sheets for Toshiba's TMPN3150B1 and Motorola's MC143150B1 for guaranteed timing specifications.

There are at least five critical timing parameters that should be checked for an external memory device in any design that interfaces to the Neuron 3150 Chip memory bus. Each of these inequalities is written from the perspective of the memory device:

• Read Access Time: Delay from address bus input valid to data output valid

$$t_{ACC,max} \quad \leq \quad t_{CYC} - t_{AD,max} - t_{DSR,min}$$

• Read ~OE Time: Delay from ~OE input to data output valid

$$t_{OE,max} \quad \leq \quad PW_{EL,min} - t_{DSR,min} - t_{OEdecode,max}$$

• Read ~CE Time: Delay from ~CE input to data output valid

$$t_{CE,max} \quad \leq \quad t_{CYC} - t_{AD,max} - t_{DSR,min} - t_{CEdecode,max}$$

- Write Data Setup Time: Delay from data input valid to ~WE input rising

$$t_{DS,max} \quad \leq \quad PW_{EL,min} - t_{DDW,max} + t_{WEdecode,min}$$

- Write Data Hold Time: Delay from ~WE input rising to data bus not valid

$$t_{DH,max} \quad \leq \quad t_{DHW,min} - t_{WEdecode,max}$$

The time on the left of each inequality is a specification from the memory device's data sheet. The times on the right side of each inequality are from the Neuron 3150 Chip timing specifications (see table 1), along with any additional delays from external decode logic. The decoding delay $t_{OEdecode}$ is measured from the falling edge of ~E to the falling edge of ~OE. The decoding delay $t_{CEdecode}$ is measured from the time the address bus A[0..15] is stable to the falling edge of ~CE. The decoding delay $t_{WEdecode}$ is measured from the rising edge of ~E to the rising edge of ~WE.

Although the five critical timing parameters listed above are generally the hardest for an external memory device to meet, other timing parameters for a candidate external memory device also need to be checked. These include the Address Setup Time, Address Hold Time, Output Disable Time and Read Data Hold Time.

The Neuron Chip supports a maximum input clock frequency of 10MHz; this translates to a 200ns processor cycle time (t_{CYC}). To specify a read-only memory device, the inequality for t_{ACC} shows:

$$t_{ACC,max} \quad \leq \quad t_{CYC} - t_{AD,max} - t_{DSR,min}$$

$$t_{ACC,max} \quad \leq \quad 200ns - 45ns - 25ns$$

$$t_{ACC,max} \quad \leq \quad 130ns$$

Thus, a read-only memory device must have a read access time of $\leq$ 130ns for 10MHz Neuron 3150 Chip operation.   For 5MHz operation, the read access time must be $\leq$ 330ns.

RAM devices latch data on the rising edge of the write enable signal. Static RAM devices requiring a 0ns address hold time (t_{AH}) beyond write enable are easy to find, and work best for Neuron Chip external memory applications. Non-volatile SRAM modules, with their internal power-down protection logic, may demand a longer address hold time than the Neuron 3150 Chip can provide. Such devices may require external latches to extend the address hold time.

The delay between ~E and the write strobe (~WE) generated for external memory must be minimized. If there is significant delay between ~E and a write strobe, then the data and address hold times for the external memory could be violated. The data hold time (t_{DH}) and address hold time (often called t_{WR}) for external memory must be checked on the memory's data sheet. The delay of the write strobe generation gate ($t_{WEdecode,max}$) is then chosen to meet the $t_{DH,max}$ inequality listed above, and also to obey the following:

$$t_{WR,max} \quad \leq \quad t_{AH,min} - t_{WEdecode,max}$$

Depending on the type of memory, $t_{WEdecode,max}$ can usually only be a few nanoseconds, so a single AC or AS gate may be required. Sometimes more address decoding is necessary. In this case, the delayed logic decode signal should be qualified with ~E in the last gate generating the write strobe signal. Gating ~E with the logic decode signal ensures that the rising edge of the write strobe ~WE will be delayed from ~E as little as possible.

Undervoltage Reset Circuit

In order to protect the integrity of the Neuron 3150 Chip's internal EEPROM, an undervoltage reset circuit (sometimes called Low Voltage Interrupt circuit or LVI) such as the Motorola MC33164 or Dallas DS1233 is required. These circuits assert the ~Reset signal whenever the +5V power supply to the Neuron 3150 Chip drops below the LVI's threshold. This prevents the Neuron 3150 Chip from attempting to operate when the +5V supply is too low to guarantee correct operation, and provides significant protection against unintentional writes to internal EEPROM. The LVI must reliably hold ~Reset asserted low when the Vcc supply drops as low as 1.5V. The LVI must have an open-drain or open-collector ~Reset output, since the Neuron 3150 Chip also asserts ~Reset during its internally generated software resets and watchdog resets.

The second generation Neuron 3150 Chips from Motorola and Toshiba may provide an LVI function for on-chip EEPROM protection. An off-chip LVI may still be needed to ensure correct reset sequencing at power-up, to protect off-chip non-volatile memory, or as part of the transceiver ESD protection circuitry for a node. An off-chip LVI may also be needed if other circuitry on a node requires that ~Reset be asserted at a higher trip point than that provided by the on-chip LVI. Consult Motorola and Toshiba for the latest information about their on-chip LVIs, and refer to the appropriate transceiver User's Guide for more information about reset issues and ESD protection.

In addition to these basic requirements for an LVI, some memory circuits require additional ~Reset conditioning logic. NVRAM and EEPROM circuits must be protected against artificially-shortened write cycles, so the LVI ~Reset signal (from a 5% LVI) must be qualified with R/~W = high, and synchronized with the falling edge of ~E. Since this qualification logic will not reliably hold ~Reset asserted when Vcc drops as low as 1.5V, an additional LVI with a lower trip point (typically 10%) must be connected directly to the ~Reset input into the Neuron 3150 Chip.

The LVI that is used with flash memory must incorporate a pulse-stretching capability (see the Dallas DS1233 data sheet, for example). The narrow ˜Reset pulse generated by Neuron 3150 Chip during a software reset must be stretched by the LVI for longer than the flash memory sector program cycle time, which is typically 10ms. This is necessary to ensure that the Neuron 3150 Chip is able to access flash memory immediately following a reset, even if a write to flash memory was performed just before the reset.

Non-volatile Memory Design Issues

A memory interface design including non-volatile memory such as flash memory, EEPROM or NVRAM provides the ultimate in flexibility by allowing changes to non-volatile configuration variables and application code. The requirement to preserve data across critical system state transitions, such as power cycling and resets, requires special considerations that address the behavior of the external memory bus during these transitions. This section describes the types of non-volatile memories that are supported by the Neuron Chip Firmware, and the bus behavior during critical state transitions.

Starting with LonBuilder 3.0 and NodeBuilder 1.0, Echelon's development tools support the use of flash memory. In most cases, flash memory will be the best choice for downloadable external memory. Flash memory is less expensive than EEPROM, and flash memory designs are generally less expensive than battery-backed SRAM.

When writing to EEPROM, the Neuron 3150 Chip Firmware treats each byte write operation the same as a write to RAM followed by a configurable delay period for the operation to complete. The Neuron 3150 Chip Firmware uses a different algorithm to write to flash memory. This algorithm has the capability to buffer one sector of flash memory data at a time.

The flash memory sector size is 64 bytes for the Atmel AT29C256 and AT29C257, and 128 bytes for the AT29C512. When the Neuron 3150 Chip Firmware is directed to write into a flash memory region, the firmware first reads all the bytes from the sector into RAM, and then if the new data is different from the existing data, the firmware will update the RAM copy, and write the new sector data into the flash memory.

Flash memory, as well as EEPROM memory, will support only a limited number of write cycles. This is often referred to as the "endurance" of the part, and it varies depending upon a number of factors. Example 4 in this engineering bulletin discusses the issue of flash memory endurance in more detail.

A typical design that uses an EEPROM memory to store application code and constants must include a separate EPROM memory to contain the Neuron Chip Firmware. The reason for this restriction is that EEPROM devices lock out read access to memory while a write is in progress.

An externally generated reset caused by the grounding of the ~RESET pin could shorten the memory write operation and thus violate some of the timing parameters discussed earlier. A reliable design must qualify the source of an external reset with R/~W = high, and synchronize it with the falling edge of ~E.

The Neuron 3150 Chip Firmware uses a JEDEC approved Software Data Protection (SDP) mechanism to provide additional write protection for flash memory configurations over 21K bytes. Use of the SDP feature is highly recommended. Refer to the LonBuilder and NodeBuilder User's Guides for more information.

EPROM programmers that support flash memory generally have a mechanism to enable this SDP, or "Secure" mode. Consult your EPROM programmer's instruction manual for more information.

Memory Design Examples

Several examples of external memory configurations are detailed in the following sections. Each design is based on the timing parameters defined in table 1. Second generation (0.8μ) Neuron 3150 Chips are required for examples 4-6.

The latest version of this engineering bulletin is kept on Echelon's LonLink bulletin board. Before beginning a new design involving the Neuron 3150 Chip and external memory, developers should check the LonLink bulletin board to ensure that they have the latest version of the example schematics.

These designs are shown only as examples. Many other configurations are possible. Developers of LONWORKS devices based on these example memory schematics are responsible for verifying that their designs meet all timing specifications for the Neuron 3150 Chip. Board layout issues such as grounding and bypassing are very important to the proper operation of these circuits.

Example 1 - External Memory Interface with 32K x 8 EPROM

Example 1 represents a minimum configuration using 32K bytes of external EPROM memory. This design supports a wide range of applications where the RAM requirement is less than the 2K bytes of internal RAM. The Neuron 3150 Chip requires 16K bytes of the external EPROM memory to contain the Neuron Chip Firmware. The remaining 16K bytes of external EPROM space is available for application code and constants.

Using the timing parameters for a 10MHz Neuron 3150 Chip and a Microchip 27C256-12 EPROM (Vcc = 5V±10%, T=-40C to 85C), the five critical timing inequalities for the example schematic can be verified:

- Read Access Time:

$$t_{ACC,max} \leq t_{CYC} - t_{AD,max} - t_{DSR,min}$$

$$120ns \leq 200ns - 45ns - 25ns$$

$$120ns \leq 130ns$$

- Read ~OE Time:

$$t_{OE,max} \leq PW_{EL,min} - t_{DSR,min} - t_{OEdecode,max}$$

$$50ns \leq 95ns - 25ns - 0ns$$

$$50ns \leq 70ns$$

- Read ~CE Time:

$$t_{CE,max} \leq t_{CYC} - t_{AD,max} - t_{DSR,min} - t_{CEdecode,max}$$

$$120ns \leq 200ns - 45ns - 25ns - 0ns$$

$$120ns \leq 130ns$$

- Write Data Setup Time: Not Applicable for EPROM

- Write Data Hold Time: Not Applicable for EPROM

At 5MHz, an EPROM with 330ns access time is sufficient, as long as the other timing requirements are satisfied.

Suitable EPROM and one-time programmable (OTP) devices are listed at the end of this document. To reduce node cost for large-volume production, masked ROM devices can be substituted for the EPROM.

The data file needed to program the EPROM is created by LonBuilder and NodeBuilder in either Motorola S-record or Intel hex format by exporting a Neuron ROM Image (.NRI) file.
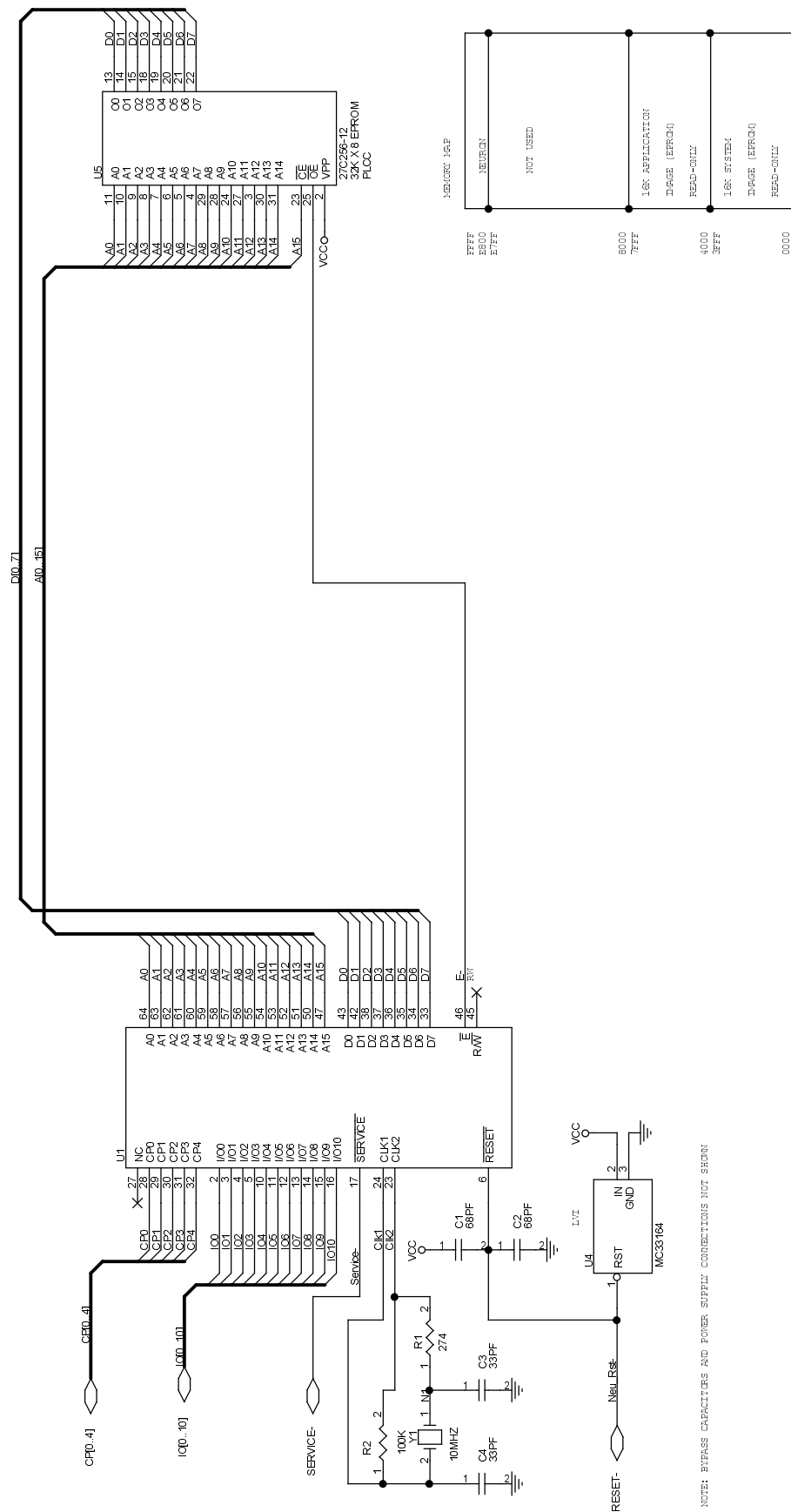
U5
27C256-12
32K X 8 EPROM
PLCC

Pin	Signal		Pin	Signal
13	D0	O0	11	A0	A0
14	D1	O1	10	A1	A1
15	D2	O2	9	A2	A2
18	D3	O3	8	A3	A3
19	D4	O4	7	A4	A4
20	D5	O5	6	A5	A5
21	D6	O6	5	A6	A6
22	D7	O7	4	A7	A7

D[0..7]

A[0..15]

MEMORY MAP

Address	Region
FFFF E800 E7FF	NEURON
	NOT USED
8000 7FFF	16K APPLICATION IMAGE (EPROM) READ-ONLY
4000 3FFF	16K SYSTEM IMAGE (EPROM) READ-ONLY
0000	

EXAMPLE #1 - 32K EPROM

CP[0..4]

IO[0..10]

SERVICE-

RESET-

NOTE: BYPASS CAPACITORS AND POWER SUPPLY CONNECTIONS NOT SHOWN

C1 68PF

C2 68PF

R1 274

C3 33PF

R2 100K

Y1 10MHZ

C4 33PF

U4 MC33164
RST IN
GND

Neu Rst-

Example 2 - External Memory Interface with 32K x 8 EPROM and I/O Expansion

Example 2 shows the addition of memory-mapped I/O to the basic EPROM circuit from example 1. The HC259 addressable latch is used to store a byte of output data (written one bit at a time by the Neuron 3150 Chip). The HC244 is used to buffer a byte of input data.

Using the timing parameters for a 10MHz Neuron 3150 Chip and the HC244/259 parts (Vcc = 5V±10%, T=-40C to 85C), the five critical timing inequalities for the example schematic can be verified:

• Read Access Time (HC244): Not Applicable -- See $t_{OE,max}$

• Read ~OE Time (HC244):

$t_{OE,max} \quad \leq \quad PW_{EL,min} - t_{DSR,min} - t_{OEdecode,max}$

$50ns \quad \leq \quad 95ns - 25ns - (1)(8.5ns)$

$50ns \quad \leq \quad 61.5ns$

• Read ~CE Time (HC244): Not Applicable -- See $t_{OE,max}$

• Write Data Setup Time (HC259):

$t_{DS,max} \quad \leq \quad PW_{EL,min} - t_{DDW,max} + t_{WEdecode,min}$

$25ns \quad \leq \quad 95ns - 60ns + (1)(0ns)$

$25ns \quad \leq \quad 35ns$

• Write Data Hold Time (HC259):

$t_{DH,max} \quad \leq \quad t_{DHW,min} - t_{WEdecode,max}$

$0ns \quad \leq \quad 9ns - (1)(8.5ns)$

$0ns \quad \leq \quad 0.5ns$

Note that the worst case gate delay is 8.5ns for the AC32.

Instead of using discrete parts for the memory devices and memory-mapped I/O devices, the PSD3xx Programmable Peripheral ICs available from WSI offer a one chip alternative. These parts contain ROM/EPROM, RAM, memory-mapped I/O and some decoding logic in a single IC. See the section on *Related Documentation* earlier in this engineering bulletin for more information on this family of parts.
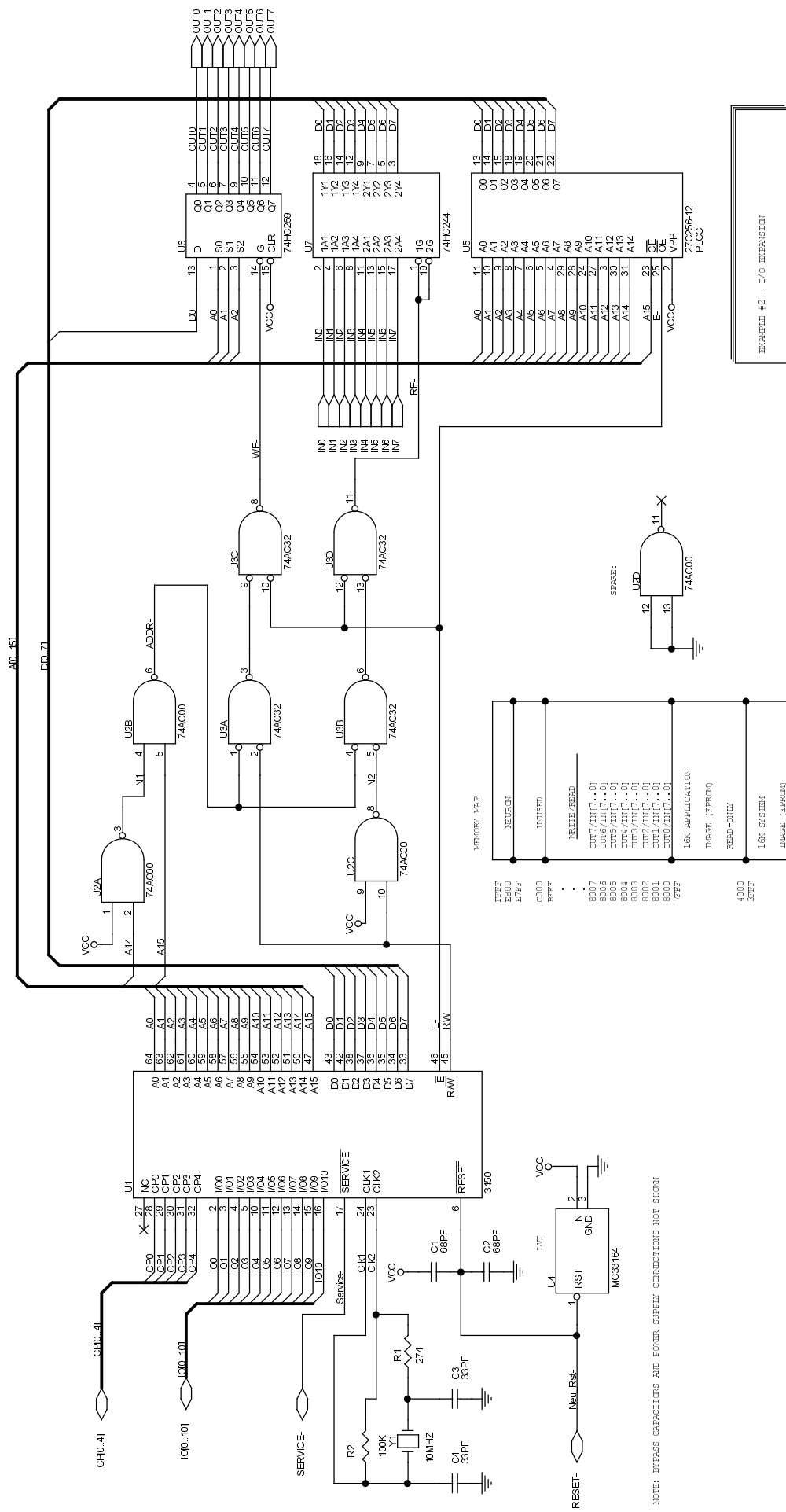
EXAMPLE #2 - I/O EXPANSION

NOTE: BYPASS CAPACITORS AND POWER SUPPLY CONNECTIONS NOT SHOWN

Example 3 - External Memory Interface with 32K x 8 EPROM and 24K x 8 SRAM

Example 3 shows a design that adds a 32K x 8 static RAM part to the basic 32K x 8 EPROM design shown in example 1. Applications requiring more than the 2K bytes of internal RAM require such an external SRAM device.

This design addresses the requirements of RAM intensive applications by providing 24K bytes of addressable external SRAM. Memory overlap with the Neuron 3150 Chip internal address space reduces the total available RAM from 32K to 26K, and the simplified address decoding shown in this example addresses only 24K. Since the SRAM is volatile, no code can be kept in it.

The Neuron 3150 Chip reserves the upper 6K bytes of address space (0xE800-0xFFFF) for internal memory. When the Neuron 3150 Chip reads from this address range, the external data bus may be driven with the internally read data. If an external memory device is enabled in this address range, bus contention will occur. This example design prevents contention by including logic to de-select the external RAM for address 0xE000 and above. The external 24K SRAM memory is therefore mapped to the address range 0x8000-0xDFFF, and the upper 8K bytes of the SRAM part are unused.

The timing of the EPROM memory interface is identical to that described for example 1. The five critical timing parameters are verified below for the Toshiba TC55257CFL-70L SRAM (Vcc = 5V±10%, T=0C to 70C) in the 10MHz design shown in the schematic:

- Read Access Time:

$$t_{ACC,max} \leq t_{CYC} - t_{AD,max} - t_{DSR,min}$$
$$70ns \leq 200ns - 45ns - 25ns$$
$$70ns \leq 130ns$$

- Read ~OE Time:

$$t_{OE,max} \leq PW_{EL,min} - t_{DSR,min} - t_{OEdecode,max}$$
$$35ns \leq 95ns - 25ns - 0ns$$
$$35ns \leq 70ns$$

- Read ~CE Time:

$$t_{CE,max} \leq t_{CYC} - t_{AD,max} - t_{DSR,min} - t_{CEdecode,max}$$
$$70ns \leq 200ns - 45ns - 25ns - (2)(8.0ns)$$
$$70ns \leq 114ns$$

- Write Data Setup Time:

$$t_{DS,max} \leq PW_{EL,min} - t_{DDW,max} + t_{WEdecode,min}$$
$$30ns \leq 95ns - 60ns + (1)(0ns)$$

30ns   ≤   35ns

• Write Data Hold Time:

$t_{DH,max}$ ≤ $t_{DHW,min}$ - $t_{WEdecode,max}$

0ns   ≤   9ns - (1)(8.5ns)

0ns   ≤   0.5ns

Note that the worst case gate delay is 8.0ns for the AC00, and 8.5ns for the AC32. Suitable SRAM devices are listed at the end of this bulletin.

EXAMPLE #3 - 32K EEROM/24K SRAM

U6
TC55257CFL
32K X 8 SRAM
PLCC

D0 D1 D2 D3 D4 D5 D6 D7
11 12 13 15 16 18 19

IO0 IO1 IO2 IO3 IO4 IO5 IO6 IO7

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14
10 9 7 6 5 4 25 24 21 23 2 26 1

CE
OE
WR

CE- 20 22
E-   22
WE- 27

U5
27C256-12
32K X 8 EEROM
PLCC

D0 D1 D2 D3 D4 D5 D6 D7
13 14 15 18 19 20 21 22

O0 O1 O2 O3 O4 O5 O6 O7

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15
11 10 8 6 5 4 29 28 24 3 31 23 25 2

CE
OE
VPP

VCCO

A[0..15]
D[0..7]

CE- U2B 6 74AC00 4 5
WE- U3A 3 74AC32 1 2

U2A 74AC00 1 2 3

A13
A14
A15

SPARE
U3B 74AC32 4 5 6
U3C 74AC32 4 5 8
U3D 74AC32 9 10 11
U2C 74AC00 12 13 11
U2D 74AC00 12 13

MEMORY MAP

NEURON   FFFF EB00 E7FF
UNUSED   E000 DFFF
24K SRAM   8000 7FFF
16K APPLICATION EEROM (EIPROM) READ-ONLY   4000 3FFF
16K SYSTEM   EEROM (EIPROM) READ-ONLY   0000

U1
3150

NC 27
CP0 28
CP1 29
CP2 30
CP3 31
CP4 32

I/O0 1
I/O1 2
I/O2 3
I/O3 4
I/O4 10
I/O5 11
I/O6 12
I/O7 13
I/O8 14
I/O9 15
I/O10 16

SERVICE 17
CLK1 24
CLK2 23
RESET 6

A0 64
A1 63
A2 62
A3 61
A4 60
A5 59
A6 58
A7 57
A8 56
A9 55
A10 54
A11 53
A12 52
A13 51
A14 50
A15 47

D0 43
D1 42
D2 38
D3 37
D4 36
D5 35
D6 34
D7 33

E- 46
R/W 45

CP[0..4]
I/O[0..10]
SERVICE-
Neu Rst-
RESET-

CP0 CP1 CP2 CP3 CP4
I/O0 I/O1 I/O2 I/O3 I/O4 I/O5 I/O6 I/O7 I/O8 I/O9 I/O10

Service-
Clk1
Clk2

VCC
C1 68PF
C2 68PF

R1 274
R2 100K
C3 33PF
C4 33PF
Y1 10MHZ

U4
MC33164
RST 1
IN 2
GND 3
LVI
VCC

NOTE: BYPASS CAPACITORS AND POWER SUPPLY CONNECTIONS NOT SHOWN

Example 4 - External Memory Interface with 32K x 8 Flash Memory

Example 4 shows a single flash memory part serving as the entire external memory for the Neuron 3150 Chip. The lower 16K of this part must have the Neuron Chip Firmware loaded into it using an EPROM programmer. The upper 16K of this flash memory can either be loaded by an EPROM programmer, or it can be loaded by a development tool or network management tool over the network. EPROM programmers that support flash memory generally have a mechanism to enable the Software Data Protection (SDP) mode, or "Secure" mode. Consult your EPROM programmer's instruction manual for more information.

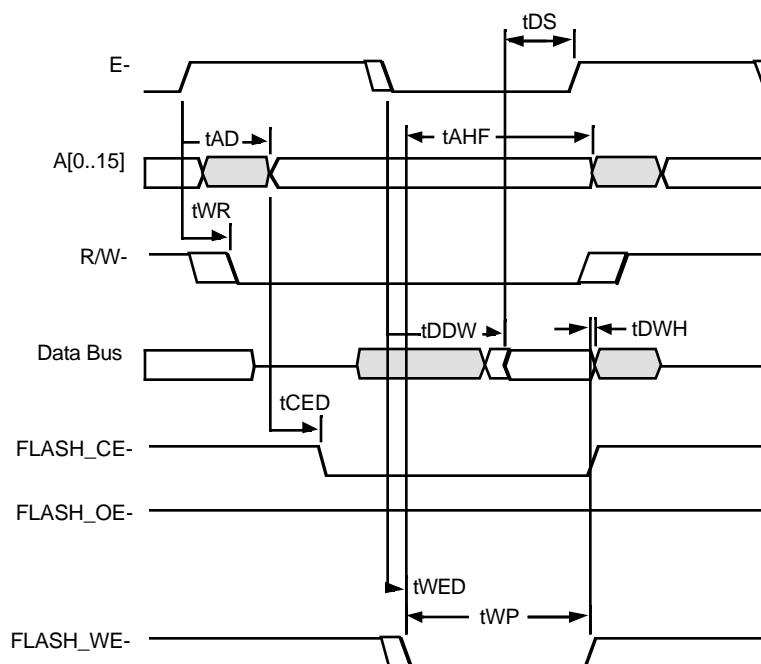The timing diagrams for flash memory write and read cycles are given in figure 3 and figure 4 below.

Figure 3 Flash Memory Write Cycle Timing

At present, only Atmel's flash memories are approved for use with Neuron 3150 Chips. Note that Atmel's standard flash memories no longer require a selection code for $t_{DS} \geq 35ns$. The AT29C256/257/512/010 parts now specify $t_{DS} \geq 35ns$ across all speeds, packages and temperature ranges (their old specification was $t_{DS} \geq 50ns$). Atmel's data sheets for these parts are being revised to reflect this change.
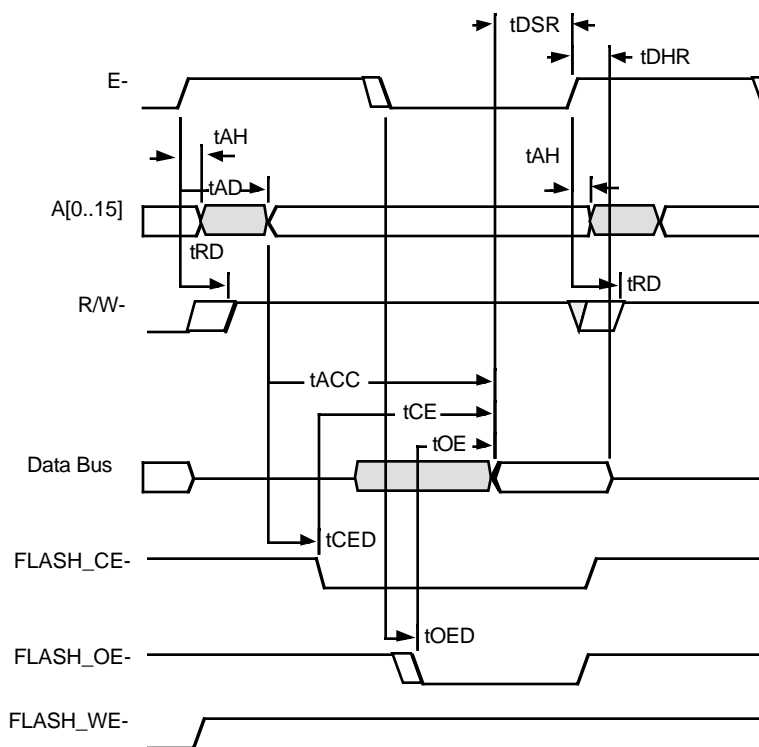
Figure 4 Flash Memory Read Cycle Timing

The five critical timing parameters are verified below for the Atmel AT29C257-120JC flash memory (Vcc = 5V±10%, T=0C to 70C) in the 10MHz design shown in the schematic:

- Read Access Time:

$t_{ACC,max}$	$\leq$	$t_{CYC} - t_{AD,max} - t_{DSR,min}$
120ns	$\leq$	200ns - 45ns - 25ns
120ns	$\leq$	130ns

- Read ~OE Time:

$t_{OE,max}$	$\leq$	$PW_{EL,min} - t_{DSR,min} - t_{OEdecode,max}$
50ns	$\leq$	95ns - 25ns - (1)(8.5ns)
50ns	$\leq$	61.5ns

- Read ~CE Time:

$t_{CE,max}$	$\leq$	$t_{CYC} - t_{AD,max} - t_{DSR,min} - t_{CEdecode,max}$
120ns	$\leq$	200ns - 45ns - 25ns - 0ns
120ns	$\leq$	130ns

- Write Data Setup Time:

$$t_{DS,max} \quad \leq \quad PW_{EL,min} - t_{DDW,max} + t_{WEdecode,min}$$

$$35ns \quad \leq \quad 95ns - 60ns + (1)(0ns)$$

$$35ns \quad \leq \quad 35ns$$

- Write Data Hold Time:

$$t_{DH,max} \quad \leq \quad t_{DHW,min} - t_{WEdecode,max}$$

$$0ns \quad \leq \quad 9ns - (1)(8.5ns)$$

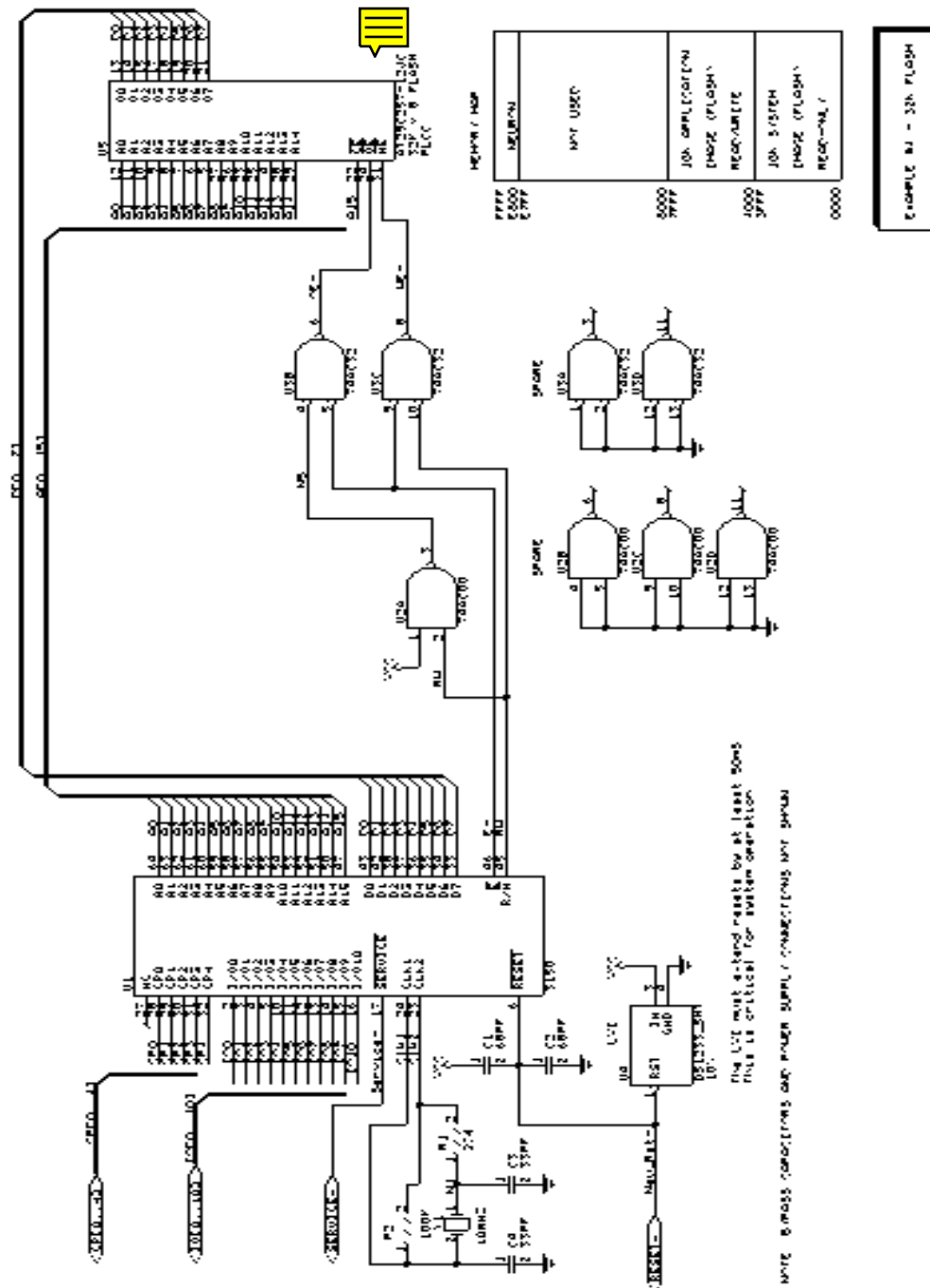$$0ns \quad \leq \quad 0.5ns$$

The worst case gate delay is 8.0ns for the AC00, and 8.5ns for the AC32. Note that the address hold time for write cycles required by these Atmel flash memory devices is $t_{AHF} \geq 50ns$, measured from the falling edge of the write strobe ~WE (see figure 3). The specification for $t_{AH} = 10ns$ that is guaranteed by the Neuron 3150 Chip is measured from the rising edge of ~E (see figure 2). The address hold time required by the Atmel flash memory parts is met by the Neuron 3150 Chip when the appropriate edge of ~WE is used for the comparison.
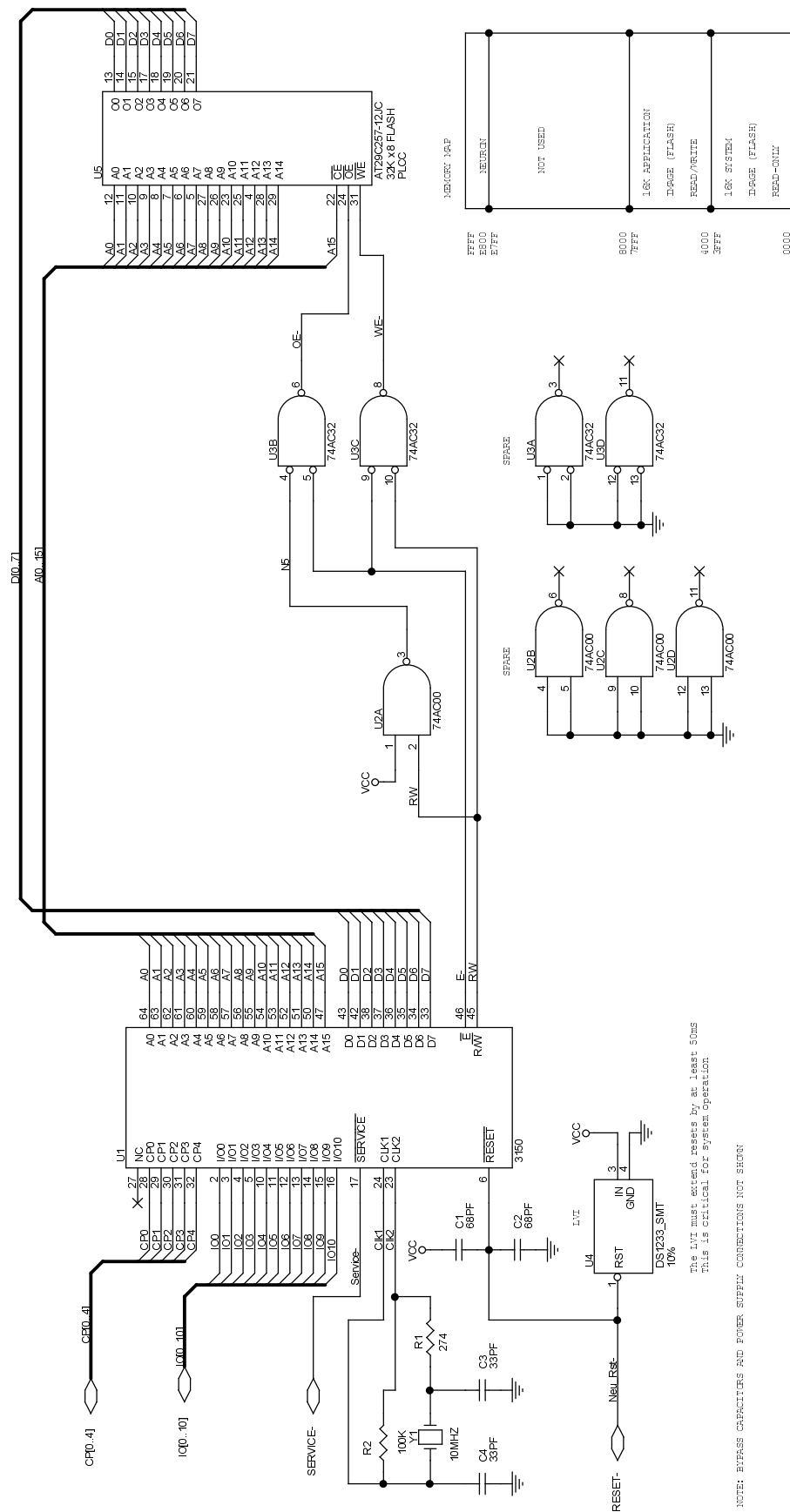
A designer of LONWORKS devices containing flash memory should keep in mind that flash memory parts have a limited endurance in terms of the number of write cycles performed on the part. The maximum number of write cycles depends on the part, and on the temperature range that the part is operated over. Consult the manufacturer's data sheet for endurance information.

In order to estimate endurance, it is important to understand how the version 6 firmware in the Neuron 3150 Chip handles writes to flash memory. When the Neuron 3150 Chip Firmware is directed to write into a flash memory region, the firmware first reads all the bytes from the appropriate flash memory sector into RAM, and then if the new data is different from the existing data, the firmware will update the RAM copy, and write the new sector data into the flash memory. If the firmware has an entire block of information to update in the flash memory, then it will do multiple writes into its RAM copy of the sector before writing the sector to the flash memory.

However, when write memory commands are received by the Neuron 3150 Chip over the network, these commands typically contain only 11-16 bytes of data to be updated (depending on the source of the write memory command). Since the sector size of the AT29C256/257 is 64 bytes, several write cycles will be performed on a sector by the Neuron Chip Firmware if 11 byte write memory commands are used over the network to write the whole sector. This type of network management command is commonly used for loading application code by development tools and network management tools. If a 64 byte sector is completely overwritten using 11 byte network management memory write commands, then that sector will experience up to seven erase/write cycles.

Flash memory requires a pulse-stretching LVI to ensure that the reset pulse is longer than the sector program cycle time. A Dallas DS1233-10 is shown in the schematic.

EXAMPLE #4 - 32K FLASH

MEMORY MAP

FFFF EB00 E7FF	NEURON
8000 7FFF	NOT USED
4000 3FFF	16K APPLICATION PAGE (FLASH) READ/WRITE
0000	16K SYSTEM PAGE (FLASH) READ-ONLY

AT29C257-12JC
32K x8 FLASH
PLCC

U5

74AC32 U3B
74AC32 U3C
74AC00 U2A

SPARE U3A 74AC32
       U3D 74AC32

SPARE U2B 74AC00
       U2C 74AC00
       U2D 74AC00

U1
3150

DS1233_SMT
10%
U4 LVI

C1 68PF
C2 68PF
C3 33PF
C4 33PF
R1 274
R2 100K
Y1 10MHZ

CP[0..4]
IO[0..10]
SERVICE-
RESET-

D[0..7]
A[0..15]

The LVI must extend resets by at least 50ms
This is critical for system operation

NOTE: BYPASS CAPACITORS AND POWER SUPPLY CONNECTIONS NOT SHOWN

Example 5 - External Memory Interface with 56K x 8 Flash Memory

Example 5 shows a design that is similar to example 4, but with a larger 64K byte flash memory part and more complex address decoding to access 56K out of the possible 58K external memory address space. See the discussion of flash memory timing, lifetime and LVI issues in example 4.

Since the address decoding logic used to generate the ~CE input to the flash memory is different from example 4, the five critical timing parameters must be verified again. They are listed below for the Atmel AT29C512-90JC flash memory (Vcc = 5V±10%, T=-40C to 85C) in the 10MHz design shown in the schematic. A 90ns flash memory part is required in this design because of the extra ~CE decoding logic that is necessary to limit the flash memory map to locations below 0xE7FF. The circuit shown in example 4 was able to use a 120ns flash memory part because A15 could be used for ~CE directly.

- Read Access Time:

$$t_{ACC,max} \leq t_{CYC} - t_{AD,max} - t_{DSR,min}$$

$$90ns \leq 200ns - 45ns - 25ns$$

$$90ns \leq 130ns$$

- Read ~OE Time:

$$t_{OE,max} \leq PW_{EL,min} - t_{DSR,min} - t_{OEdecode,max}$$

$$40ns \leq 95ns - 25ns - (1)(8.5ns)$$

$$40ns \leq 61.5ns$$

- Read ~CE Time:

$$t_{CE,max} \leq t_{CYC} - t_{AD,max} - t_{DSR,min} - t_{CEdecode,max}$$

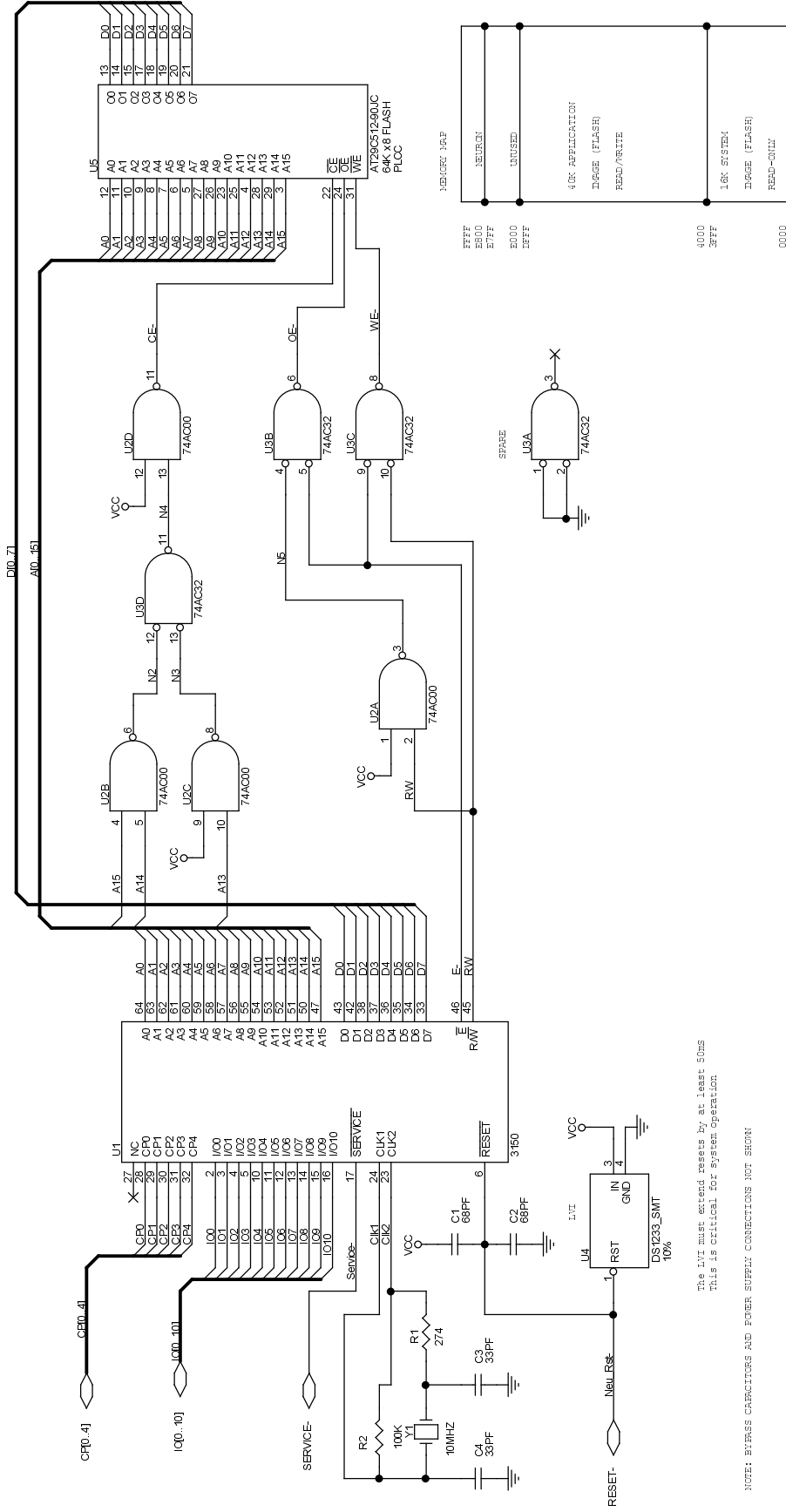$$90ns \leq 200ns - 45ns - 25ns - [(2)(8.0ns) + (1)(8.5ns)]$$

$$90ns \leq 105.5ns$$

- Write Data Setup Time:

$$t_{DS,max} \leq PW_{EL,min} - t_{DDW,max} + t_{WEdecode,min}$$

$$35ns \leq 95ns - 60ns + (1)(0ns)$$

$$35ns \leq 35ns$$

- Write Data Hold Time:

$$t_{DH,max} \leq t_{DHW,min} - t_{WEdecode,max}$$

$$0ns \leq 9ns - (1)(8.5ns)$$

$$0ns \leq 0.5ns$$

Note that the worst case gate delay is 8.0ns for the AC00, and 8.5ns for the AC32.

EXAMPLE #5 - 56K FLASH

AT29C512-90JC
64K x8 FLASH
PLCC
U5

MEMORY MAP

FFFF NEURON
EB00
EAFF UNUSED
E000
DFFF
      40K APPLICATION
      IMAGE (FLASH)
      READ/WRITE

4000 16K SYSTEM
3FFF IMAGE (FLASH)
      READ-ONLY
0000

74AC00 U2D
74AC32 U3B
74AC32 U3C
74AC32 U3A SPARE
74AC32 U3D
74AC00 U2B
74AC00 U2C
74AC00 U2A

CE-
OE-
WE-
RW

D[0..7]
A[0..15]

U1
3150

NC
CP0
CP1
CP2
CP3
CP4

I/O0
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
I/O7
I/O8
I/O9
I/O10

SERVICE
CLK1
CLK2
RESET

A0-A15
D0-D7
E-
R/W

CP[0..4]
I/O[0..10]
SERVICE-
RESET-
Neu_Rst-

VCC

C1 68PF
C2 68PF
C3 33PF
C4 33PF
R1 274
R2 100K
Y1 10MHZ

U4 DS1233_SMT 10%
LVI
IN
GND
RST

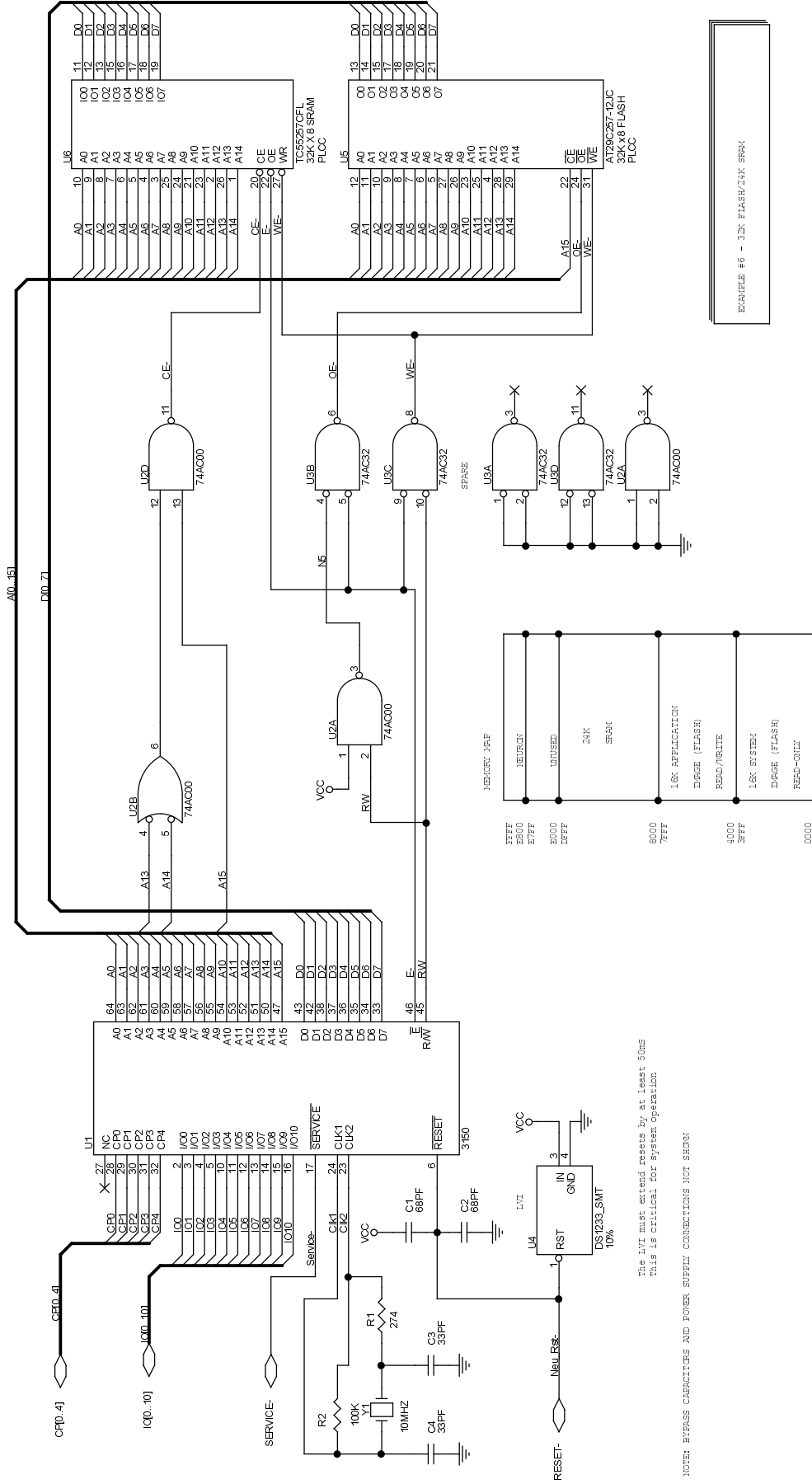The LVI must extend resets by at least 50ms
This is critical for system operation

NOTE: BYPASS CAPACITORS AND POWER SUPPLY CONNECTIONS NOT SHOWN

Example 6- External Memory Interface with 32K x 8 Flash and 24K x 8 SRAM

Example 6 shows a combination of flash memory and RAM extension. The 32K flash memory uses A15 from the Neuron Chip as its CE input, while the CE for the SRAM involves decoding the window from 0x8000-0xDFFF. More complex decoding for the SRAM could provide access to the last 2K from 0xE000-0xE7FF, in order to obtain a maximum of 26K SRAM above the flash memory.

See the discussions of SRAM and flash memory issues discussed in the earlier examples. The five critical timing parameters are verified for this flash memory configuration in example 4, and for this SRAM configuration in example 3.

EXAMPLE #6 - 32K FLASH/24K SRAM

U6
TC55257CFL
32K X 8 SRAM
PLCC

U5
AT29C257-12JC
32K x 8 FLASH
PLCC

MEMORY MAP

	NEURON
FFFF	
EB00	UNUSED
E7FF	
E000	
DFFF	24K
	SRAM
8000	
7FFF	16K APPLICATION
	PAGE (FLASH)
	READ/WRITE
4000	16K SYSTEM
3FFF	PAGE (FLASH)
	READ-ONLY
0000	

U1
3150

DS1233_SMT
10%

The LVI must extend resets by at least 50ms
This is critical for system operation

NOTE: BYPASS CAPACITORS AND POWER SUPPLY CONNECTIONS NOT SHOWN

CP[0..4]

IO[0..10]

SERVICE-

RESET-

74AC00

74AC32

SPARE

74AC32   74AC32   74AC00
U3A   U3D   U2A

R1 274
R2 100K
C1 68PF
C2 68PF
C3 33PF
C4 33PF
10MHZ
Y1

Access to Echelon's LonLink Bulletin Board

The LonLink bulletin board can be reached at the following direct dial telephone number: 1-415-856-7538. Alternately, the bulletin board can be reached through the following FTP site on the Internet: lonworks.echelon.com. Engineering bulletins can be downloaded from the bulletin board. These bulletins are viewed using Common Ground viewer software, which can also be downloaded.

The LonLink bulletin board can be reached from Telnet at lonlink.echelon.com. However, Telnet does not support file transfer.

Suitable Memory Devices

The following tables list vendors whose product lines include parts meeting the interface specifications of the Neuron 3150 Chip. The list does not cover all possible parts or semiconductor manufacturers. Contact the individual manufacturers or their representatives for price and availability.

PROM Devices (32K X 8)

Microchip	27HC256-90
Catalyst	CAT27HC256L-12
Wafer Scale Integration	WS27C256L-12J
Toshiba	TC57H256D-120
AMD	AM27C256-120JC
Atmel	AT27C256R-12JC

Static RAM Devices

Toshiba	TC55257-70L

Flash Memory Devices

Atmel	AT29C256-90, AT29C256-12
	AT29C257-90, AT29C257-12
	AT29C512-90, AT29C512-12

ECHELON