AN98491

Recommended PCB Routing Guidelines for a Cypress e.MMC Memory Device

AN98491 provides general routing guidelines for PCBs designed with a Cypress e.MMC memory device.

1 Introduction

This application note provides general routing guidelines for PCBs (printed circuit board) designed with a Cypress® e.MMC memory device. It does not eliminate the need for customer signal integrity/power delivery simulations and should be used as an initial reference towards PCB design with a Cypress e.MMC memory device. Customers should utilize Cypress provided IBIS models for signal timing/crosstalk simulations.

If customers cannot meet or beat the recommendations in this application note, detailed simulations should be performed to determine whether the exceptions would impact bus performance.

This document applies to the following Cypress devices:

- S4041XXX1B1 e.MMC series

2 Signal Descriptions

Table 1 describes various pins (and their function) used in S4041-1B1 e.MMC memory device.

Table 1. Pin Description

Pin Name	Type	Description
DAT0 - DAT7	I/O	Bidirectional data channels used for data transfers.
CMD	I/O	Bidirectional command channel used for device initialization and command transfers.
CLK	Input	Clock input.
RST_N	Input	Hardware reset.
VCC	Power	Supply voltage for the flash memory.
VCCQ	Power	Supply voltage for the memory controller and MMC interface.
VDDI	Power	Internal power node. Connect capacitor to ground.
VSS	Power	Ground pin for the flash memory.
VSSQ	Power	Ground pin for the memory controller and MMC interface.
NC	—	Not connected.
RFU	—	Reserved for future use. Do not connect.

3 Package Breakout Routing Recommendations

Figure 1. FBGA 153 (Top View, Balls Down)

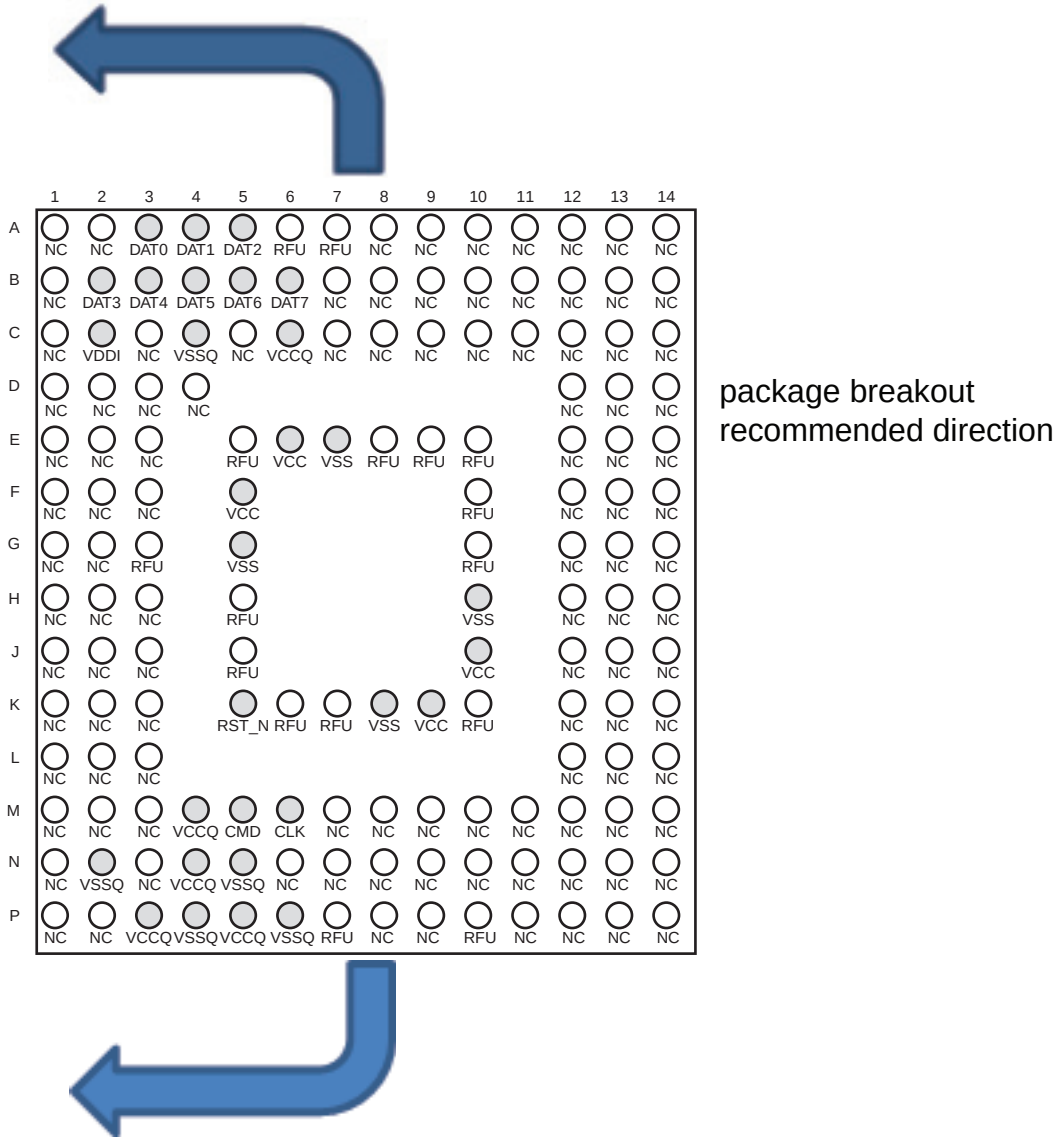
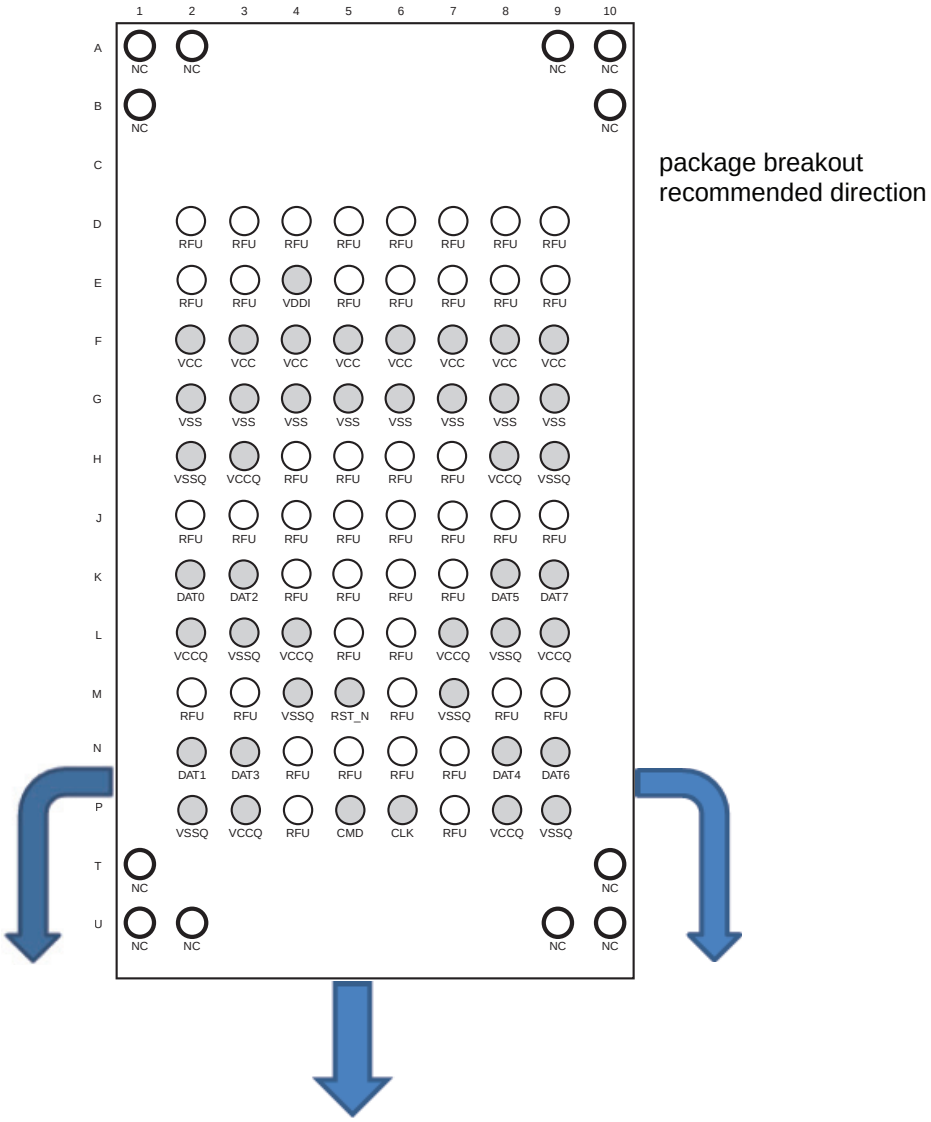


Figure 2. BGA 100 (Top View, Balls Down)



For the FBGA 153-ball package (Figure 1), a westward breakout is recommended to achieve the best length matching and shortest distance to the host controller. The supply balls can be connected to vias between the ball matrix (on PCB) to connect the PWR/GND layers.

For the BGA 100-ball package (Figure 2), a southward breakout is recommended to achieve the best length matching and shortest distance to the host controller.

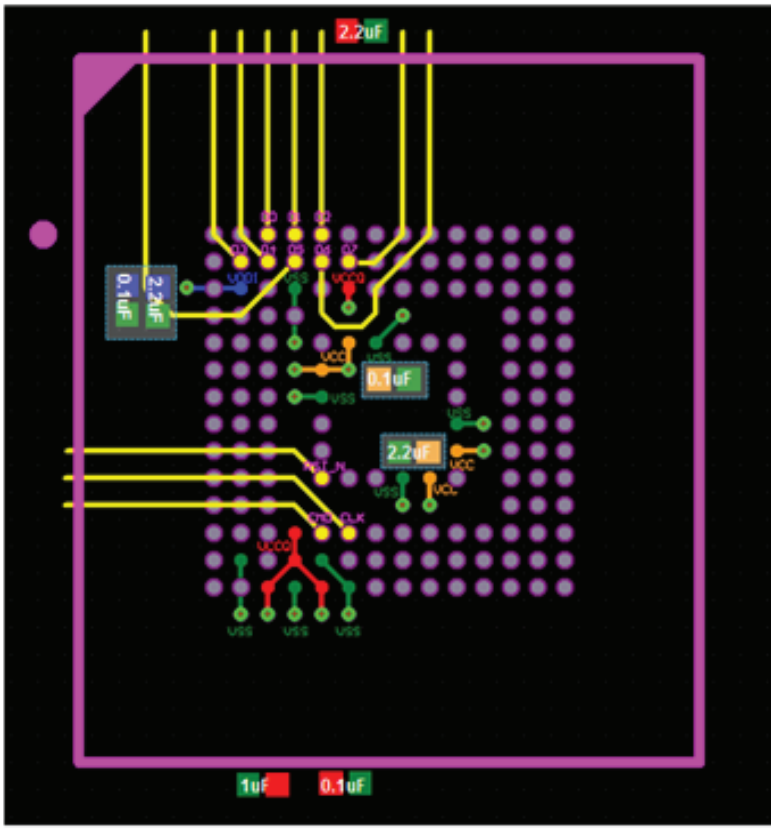
During PCB breakout, use as below:

- BGA100:
  - Ball pad size: 0.35
  - SRO size: 0.5
- BGA153:
  - Ball pad size: 0.25
  - SRO size: 0.35

Once the ball field is cleared, customers can redirect the traces in the direction of the Host controller package while maintaining a minimum 4 mil or better spacing between traces.

3.1 Top Layer Only PCB Breakout Options

Figure 3. FBGA 153 BALLMAP (Top view, balls down)
Top layer only PCB breakout recommendation



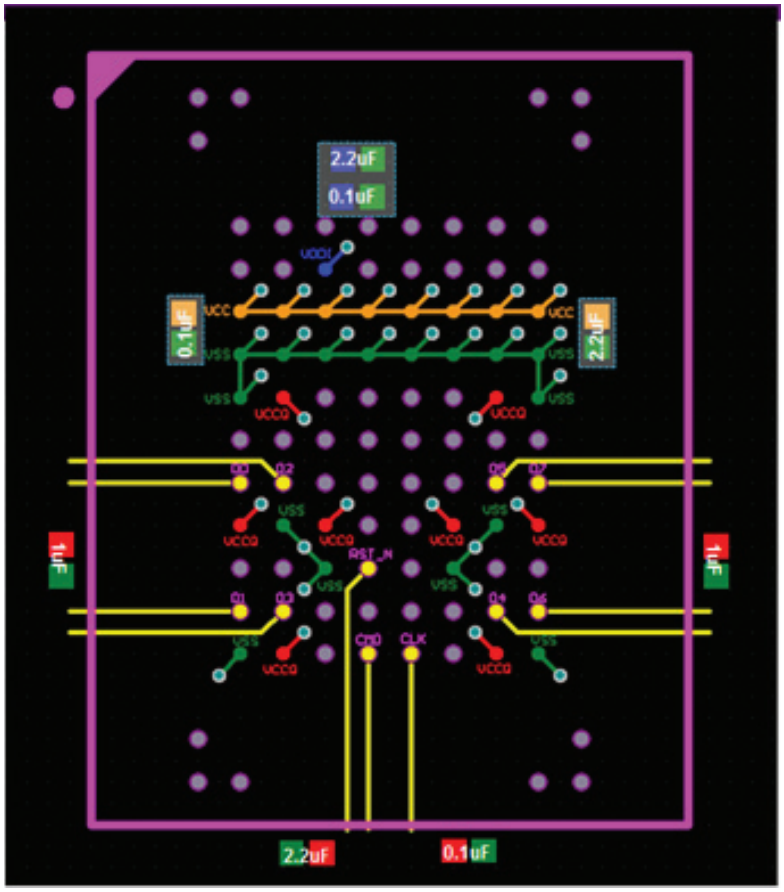
Recommended decoupling capacitors:

- VCCQ ≥ 0.1 µF x1
  2.2 µF x1 (this cap should be as close as possible to the C6 ball)
  1 x 1 µF
- VCC ≥ 0.1 µF x1 and 2.2 µF x1
- VDDi ≥ 0.1 µF x1 and 2.2 µF x1

Capacitors that are placed in the backplane are noted with a dotted line

Legend	Description
	VDDI Power Rail
	VCCQ Power Rail
	VCC Power Rail
	VSS Plane

Figure 4. FBGA 100 BALLMAP (Top view, balls down)
Top layer only PCB breakout recommendation



Recommended decoupling capacitors:

- VCCQ ≥ 0.1 µF x1
  2.2 µF x1
  2 x 2 µF
- VCC ≥ 0.1 µF x1 and 2.2 µF x1
- VDDi ≥ 0.1 µF x1 and 2.2 µF x1

Capacitors that are placed in the backplane are noted with a dotted line

Legend	Description
	VDDI Power Rail
	VCCQ Power Rail
	VCC Power Rail
	VSS Plane

4 Stackup Requirements

- Customer stackups can vary based on the end application, however Cypress recommends that all signal traces be well referenced to a solid GND plane.
- It is recommended to dedicate a plane layer to V_{CC}.
- The most straightforward stackup to meet the above requirements would be a minimum 6-layer stackup as shown below:
  - Top Layer: GND plane (allow signal breakout on this layer)
  - Signal
  - GND
  - V_{CC}
  - Signal
  - Bottom Layer: GND plane (allow some signal breakout on this layer)

The signal trace width and trace height from the GND plane needs to be adjusted based on signal impedance requirements.

- It is possible to reduce the layer requirement to a 4-layer PCB. However, the signal impedance needs to be met and the signals should be routed over a solid GND plane:
  - Top Layer (Signal):Add as many GND guard traces next to e.MMC signals as possible and connect to the GND plane using vias

- GND
- V_{CC}
- Bottom layer (Signal):Add as many GND guard traces next to e.MMC signals as possible and connect to the GND plane using vias

5 Power Delivery Guidelines

- It is recommend to connect V_{CC}/V_{CC}Q to the V_{CC} plane layer with µvias while maintaining the breakout trace as large as allowed by the ball pitch. A separate plane flood on the V_{CC} layer is needed for V_{CC} and V_{CC}Q supplies.
- It is recommend to connect V_{SS}/V_{SS}Q to the V_{SS} plane with µvias while maintaining the breakout trace as large as allowed by the ball pitch. V_{SS} and V_{SS}Q can be shared into one plane.
- It is recommended to keep the supply trace lengths ≤ 400 mil and the trace width ≥ 20 mil.
- The same care, as explained in the bullets above, should be taken for traces from the voltage regulator (PMIC) feeding into V_{CC} and V_{CC}Q. This will minimize the IR drop from the regulator.
- As much as possible, do not share V_{CC}/V_{CC}Q supply planes with other interfaces to avoid noise coupling. V_{SS} can be shared as long as it is a homogeneous plane.

Decoupling Capacitor Recommendations

- X7R or X5R capacitors are recommended with a rated voltage > 6.3V.
- 0603 or a smaller size is recommended.
- Pick capacitors with low ESL and ESR.
- It is important to place decoupling caps as close to the target supply balls while maintaining > 20 mil trace width for supply connections to capacitor SMT pads.

■Recommended Value and Quantity:

V_{CC}Q ≥ 0.1 µF x 1
2.2 µF x 1 (for BGA153, this cap should be as close as possible to C6 ball)
1 x 1 µF
1 x 1 µF (additional cap only for BGA100 package)
V_{CC} ≥ 0.1 µF x 1 and 2.2 µF x 1
V_{DDi} ≥ 0.1 µF x 1 and 2.2 µF x 1

Customer is requested to place all of the caps shown above. For V_{CC}Q caps, they should be located as close as possible to the V_{CC}Q/V_{SS}Q balls near the DAT0-7 signals.

6 Signal Routing Guidelines

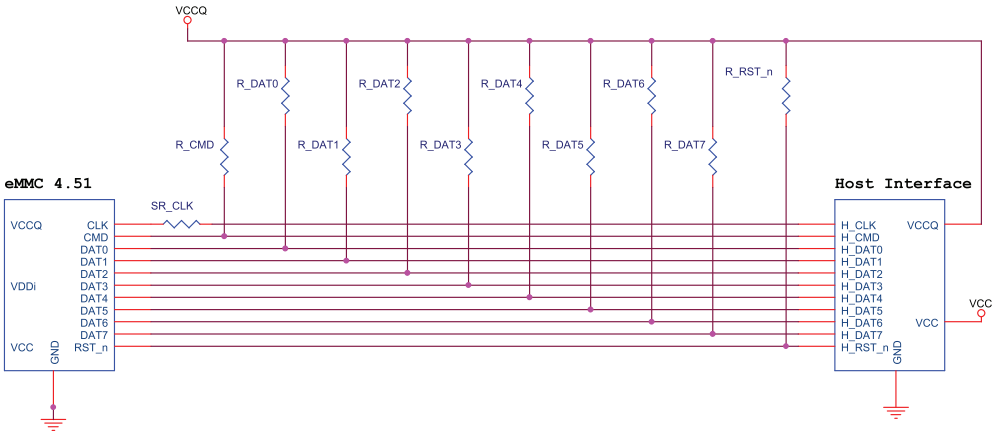
Customers are recommended to meet or beat the signal routing recommendations below.

- All length/mismatch guidelines are provided in inches. It is assumed that 1 inch is ~166 ps. Customers should use signal integrity tools to estimate the actual trace velocity and path delays to ensure that the above assumption is not violated.
- A typical 1 inch/50 ohm transmission line has a line capacitance of ~3.3 pf. While considering the total load on a line, both line length and pin capacitance values of all components connected to that line should be considered.
- Customers are encouraged to perform signal integrity simulations using Cypress provided IBIS models to determine actual guidelines suitable for their application. The guidelines below should be used as a starting reference.
- Typically, delay is measured between t_{VM} (timing reference voltage which is usually V_{CC}/2) of the source to t_{VM} of the destination. However, attention should be paid to the signal polarity in the data sheet to ensure which edge the timing is measured at (rising or falling edge).
- In general through hole vias are OK on signals as the long as board is not too thick. Otherwise these vias add impedance discontinuities and capacitance. Wherever possible use a µVia+Buried via combination.

- Either Microstrip line or Stripline is allowed for signal routing as long as trace impedance is maintained for all signals at 50 ohm ± 10%.
- Signal trace length skew constraints
  - Mismatch within DAT0~DAT7 ≤ 250 mil
  - CLK to DAT0-7 mismatch ≤ 250 mil
  - CLK to CMD mismatch ≤ 250 mil
  - CLK to RST_N mismatch ≤ 1000 mil
- Signal spacing constraints from other signals
  - CLK: > 2H
  - DS: > 2H
  - DAT0~DAT7: > 1.5H
  - CMD: > 1.5H
  - RST_N: > 1.5H

  Where H is the height of the dielectric between signal and GND (reference layer)
- Match the via count between two signals which are being considered for length matching
- CLK and DAT0-DAT7 maximum trace lengths are dependent on the following:
  - The maximum capacitive load allowed per the data sheet (1 inch ~ 3.3 pf).
  - The T_{ODLY} parameter of the e.MMC memory device.
  - The round-trip flight time due to the transmission line delays on the CLK and DAT0-DAT7 signals.
  - The input setup and hold time requirements of the e.MMC memory device.

7 Series Termination and Pull-Up Resistor Recommendations



Parameter	Symbol	Recommended	Comments
Pull-up resistance for CMD	R_CMD	10 kΩ	To prevent bus floating.
Pull-up resistance for DAT[7:0]	R_DAT	50 kΩ	To prevent bus floating.
Pull-up resistance for RST_n	R_RST_n	50 kΩ	A pull-up resistance on the RST_n (H/W reset) line is not required if the host does not enable the H/W reset feature.
Series termination for CLK	SR_CLK	22Ω	To stabilize the clock signal. It is recommend for customers to perform simulations using the controller IBIS model to confirm this value.

8 Test Points and Oscilloscope Measurements

- Test points should be added as close to the Controller for DAT0-7 and as close to the e.MMC package for all signals.
- When the controller is driving, it is meaningful to look at the signal as close to the e.MMC device as possible. When the e.MMC device is driving, the opposite is true.
- While creating a test pad, the stub resulting from the pad should be minimized. It is recommended for the customer to probe at the breakout via if the customer has the ability to do this instead of creating test pad stubs.
- While performing scope measurements, please use > 3 GHz bandwidth scope as well as a low impedance probe.
- Always measure V_{CC}-V_{SS} at the controller, voltage regulator, next to the connector (either side) and at the e.MMC device. This needs to be done prior to making any signal measurements to ensure that the supply is not noisy. A noisy supply will impact signal timing. Also, these measurements establish the IR drop from the regulator to the controller or the regulator to the e.MMC device.
- While measuring signals, it is a good idea to set the trigger on the most common switching signals such as the CLK.

9. Conclusion

This application note provides general routing guidelines for PCB's (printed circuit board) designed with a Cypress e.MMC memory device. For any questions regarding this application note, enter a support request on the Cypress support website or contact your Cypress representative.

Document History Page

Document Title: AN98491 - Recommended PCB Routing Guidelines for a Cypress e.MMC Memory Device Document Number: 001-98491				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	08/25/2014	Initial version
*A	–	–	03/02/2015	Package Breakout Routing Recommendation: FBGA 153 (Top View, Balls Down) figure: corrected ball C5 to NC Added section: Top Layer Only PCB Breakout Options Updated sections: Stackup Requirements, Power Delivery Guidelines, Signal Routing Guidelines Series Termination and Pull-Up Resistor Recommendations: Changed Comments for 'Pull-up resistance for RST_n'
*B	4943471	MSWI	09/30/2015	Updated in Cypress template

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